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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,413	02/28/2002	Brian Tse Deng	TI33539	3213

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,413	DENG ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-9,12,14,15 and 21-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,11,13 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with traverse of the species of Figs 6 A and 6B in the reply filed on 10/18/2004 is acknowledged. The traversal is on the ground(s) that "the description of FIGURES 6A, 68 starting on Page 22, Line 1, recites that the circuit of FIGURE 6 (A, B) is similar to the circuit disclosed in FIGURE 5A. Accordingly, Applicant's believe that Claims 1-21 read on the Examiner's species as the species of FIGURES 5A, 5B and 6A, 6B and could be examined at the same time." This is not found persuasive because it is irrelevant whether two different species are "similar." Rather, at issue is whether the claims are directed to patentably distinct species. As set forth in the Restriction Requirement, the species of Figs. 5(a, b) and the species of Figs. 6 (A, B) are patentably distinct. Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 1O3(a) of the other invention.

Applicants also state that claims 1-21 are readable on the species of Figs. 6 (A, B). The Examiner disagrees.

The species of Figs. 6 (A, B) does not perform the step of "decoding a debounced signal line" (claims 1-9).

The species of Figs. 6 (A, B) does not include a plurality of circuit outputs (claims 2 and 3).

The species of Figs. 6 (A, B) does not include "periodically polling the status of the signal change line (claim 4). As a matter of fact, the specification, with regard to Figs. 6(A, B), specifically discloses that "[r]ather than having to periodically test each of the signal lines and the communications bus as is commonly done to check for a change of signal or state, the peripheral controller is free to perform its tasks and when a signal line or the communications bus changes state, the independent debouncing circuit asserts a value on a single signal line to signal the controller that a change of signal or state has occurred."

The species of Figs. 6 (A, B) does not include "inputs of the subsequent storage device are also selectively coupled to the output of the memory device" (claim 12).

The species of Figs. 6 (A, B) does not include "inputs of the subsequent storage device are also selectively coupled to an output of the final storage device" (claim 14).

The species of Figs. 6 (A, B) does not include at least the "signal change flag" (claim 15).

The species of Figs. 6 (A, B) does not include at least "a decoder containing circuitry to decode a state on the communications bus and produce output should the decoded state match a desired state (claim 21).

Therefore, in addition to withdrawn claims 22-30, claims 1-9, 12, 14, 15, and 21 have also been withdrawn from further consideration, since they are directed to a non-elected species.

The requirement is still deemed proper and is therefore made **FINAL.**

Claim Rejections - 35 USC § 102

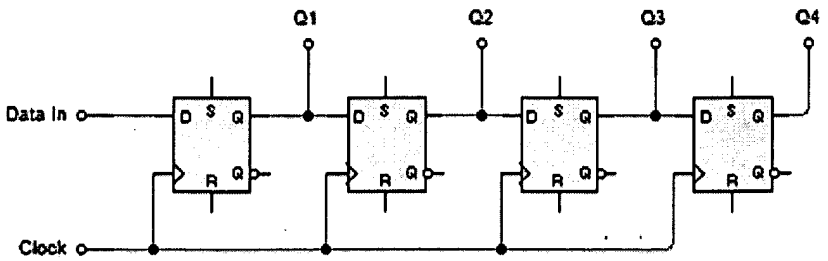
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Norris et al. (Norris, 4,523,104).

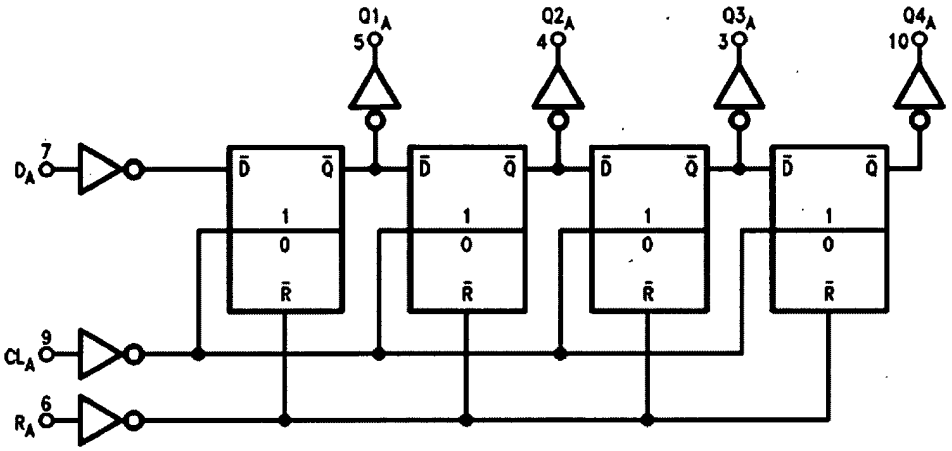
As broadly drafted, these claims do not define any structure that differs from Norris.

With regard to claim 10,Norris discloses a signal debouncing circuit (shown generally at Figs. 1 and 2; the shift register 14 of the debouncing circuit of Norris is a CD 4015 serial in-parallel out shift register. A serial in-parallel out shift register is shown below (see Wikipedia definition of a shift register, cited below):

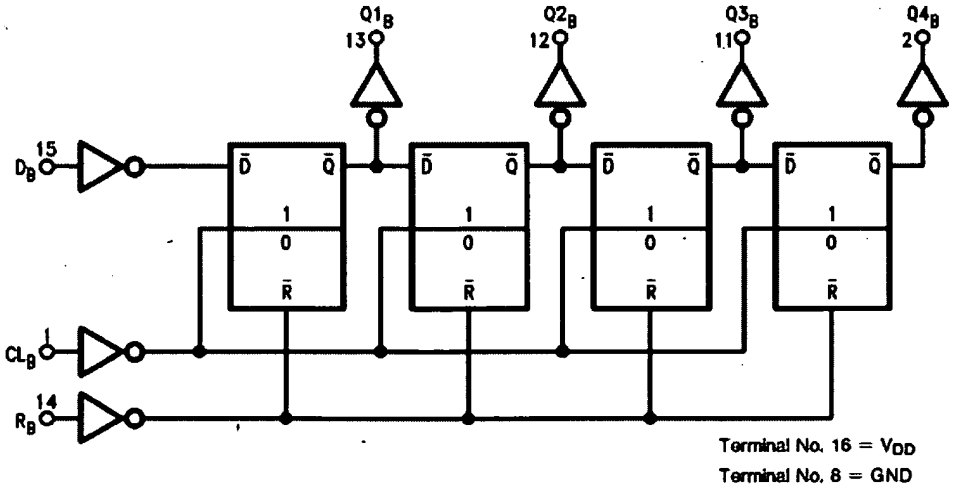


Specifically, the CD 4015 shift register of Norris is show below:

Logic Diagrams



Logic Diagrams (Continued)



(see National Semiconductor, CD4015.)

comprising: a memory device (it is clear from above that the first flip flop of the shift register 14 is readable as a memory device) coupled to a signal line, the memory device to store a value based on a signal value on the signal line (the first flip-flop of the shift register 14 stores a value based on a signal value on the signal line from the switch 12 for storing an input value); a serially connected sequence of storage devices coupled to the memory device (a series subsequent flip flops is readable as a sequence of storage devices connected to the first flip-flop), wherein: an input of a first storage device is coupled to the memory device (the flip-flop adjacent to the first flip flop is readable as a first storage device coupled to the first flip-flop); an input of subsequent storage devices is selectively coupled to an output of a previous storage device (the input of the subsequent flip-flop is selectively coupled to the output of the previous flip-flop); and an output of a last storage device provides a debounced version of the signal value provided to the memory device (it is clear from above that the last flip-flop of the shift register 14 of the debouncing circuit comprises an output to provide a debounced signal originated from the signal value provided to the first flip-flop or "memory device" of the shift register 14 of the debouncing circuit of Norris).

With regard to claim 11, it is clear that the input of subsequent storage devices or subsequent flip-flops are selectively coupled to the output of a storage device immediately before it in the sequence of storage devices (note that the sequence of storage devices are the sequence of flip-flops between the first flip-flop and the last flip-

flop of the shift register 14 of the debouncing circuit of Norris).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

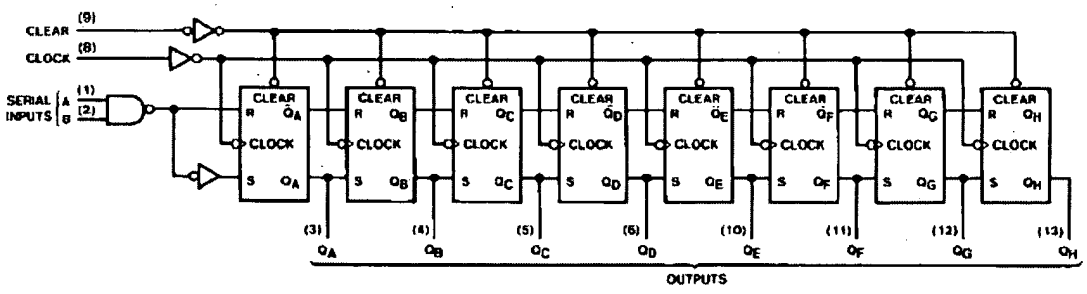
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norris et al. (Norris, 4,523,104).

Norris, as discussed above, discloses the claimed invention except that Norris does not disclose the use of additional flip-flops including the so-called "final storage device."

As noted above, the CD4015 shift register is a 4-bit shift register comprising 4 flip-flops. An 8-bit version of a shift register is shown below (see 8-bit shift register cited below):

Logic Diagram



It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an 8-bit shift register instead of a 4-bit version for the shift register 14 of the debouncing circuit of Norris, since the use 8-bit shift register vs. 8-bit shift register is only a matter of design choice depending on a particular application and a amount of data to be processed; and selecting an 8-bit shift register only involves ordinary skill in the art. As a result, since an an 8-bit shift register is used in Norris, the last flip-flop (see diagram above) is readable as a "final storage device" (claim 13). With regard to claim 16, the first two sequentially connected flip-flops (see diagram above) is readable as a "memory device." With regard to claim 17, it is clear that the flip-flops shown above are D-type flip-flops. With regard to claim 18, it is clear from the diagram above that the sequence of storage devices comprising a sequence of flip-flops. With regard to claim 19, it is clear from the diagram above that the flip-flops are D-type flip-flops. With regard to claim 20, it is from the diagram above that the final storage device is a flip-flop.

US Patent Nos. 4,549,097 to Floyd, 3,792,466 to Arnold et al., 5,386,159 to Dupre, 3,886,543 to Martin, and US PG Pub. No. 2002/0185128 to Theobald are cited as relevant art.

Floyd, Fig. 7, discloses a debouncing circuit comprising D-flip flops in combination of NAND and Exclusive OR gates. Arnold discloses a debounce circuit wherein the switch and the clock signals are applied to a shift register and the the

debounced output is obtained from a NAND gate. Dupre discloses a glitch suppressor circuit comprising D-type flip-flops, Martin discloses a debounce logic comprising shift registers and multiplexers, and Theobald discloses a plurality of debounce circuits using D- type flip-flops.

Specification of CD 4015 4-bit shift register from National Semiconductor, specification 8-bit serial in/parallel out 8-bit register from Fairchild Semiconductor, and Definition OF Shift register by Wikipedia are also cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner